IN THE CLAIMS

I claim:

Claims 1-8 (canceled):

Claim 9 (currently amended): ~~The method of claim 6, further comprising the step of performing active net tagging, after said checking step, on each of said one or more nets to determine whether any of said one or more nets will switch with regular frequency.~~

A method for statically estimating a body voltage of one or more transistors which form digital partially depleted silicon-on-insulator circuit having a predetermined circuit topology comprising said one or more transistors and one or more nets connecting said transistors, comprising the steps of:

a. obtaining one or more device models selected from the group consisting of an n channel Field Effect Transistor model and a p channel Field Effect Transistor model, each corresponding to one of said one or more transistors;

b. abstracting each of said n channel Field Effect Transistor models, if any, and each of said p channel Field Effect Transistor models, if any, to obtain one or more displacement voltages d_i, steady-state reference voltages V_i^{Zero}, and forward bias reference voltages $V_i^{forward}$, for each of said device models to generate one or more simplified electrical descriptions, each corresponding to one of said one or more transistors;

c. checking said predetermined circuit topology to generate one or more sets of accessible states, each set corresponding to one of said one or more transistors and being indicative of whether under any allowable switching activity, the source, gate or drain could be high or low;

d. performing active net tagging on each of said one or more nets to determine whether any of said one or more nets will switch with regular frequency.

e. determining one or more sets of reference state body voltage minima and reference state body voltage maxima, one for each of said one or more transistors, based on corresponding simplified electrical descriptions and corresponding sets of accessible states; and

f. ascertaining one or more target state body voltage minima and target state body voltage maxima, one for each of said one or more transistors, based on said determined sets of reference state body voltage minima and reference state body voltage maxima.

Claim 10 (original): The method of claim 9, wherein said corresponding simplified electrical descriptions comprise said displacement voltages d_i, and said determining step comprises determining said sets of reference state body voltage minima, and reference state body voltage maxima based on corresponding displacement voltages d_i, and corresponding set of accessible states, and from said determination from said active net tagging.

Claim 11 (original): The method of claim 10, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, based on said determined reference state body voltage minima and maxima using modified accessibility analysis.

Claims 12-22 (canceled).